ZHEJIANG UNIU-NE Technology CO.,LTD

浙 江 宇 力 微 新 能 源 科 技 有 限 公 司

U3406 Data Sheet

V0.5

General Description

The U3406 400V synchronous buck controller regulates from a high input voltage source or from an input rail subject to high voltage transients, minimizing the need for external surge suppression components. A high-side switch minimum on-time of 60 ns gives large step-down ratios, enabling the direct step-down conversion from a 100V nominal input to low-voltage rails for reduced system complexity and solution cost. The U3406 continues to operate during input voltage dips as low as 8.5V, at nearly 100% duty cycle if needed, making it an excellent choice for high-performance 100V battery automotive applications, ADAS (surround view ECU) and HEV/EV systems.

Forced-PWM (FPWM) operation eliminates switching frequency variation to minimize EMI, while user-selectable diode emulation lowers current consumption at light-load conditions. Measuring the voltage drop across the low-side MOSFET or with an optional current sense resistor gives cycle-by-cycle overcurrent protection. The adjustable switching frequency as high as 0.5MHz can be synchronized to an external clock source to eliminate beat frequencies in noise-sensitive applications.

Applications

- High-Power Automotive DC/DC Regulator
- Automotive Motor Drives, ADAS
- HEV/EV Power Compliant to LV-148

Key Features

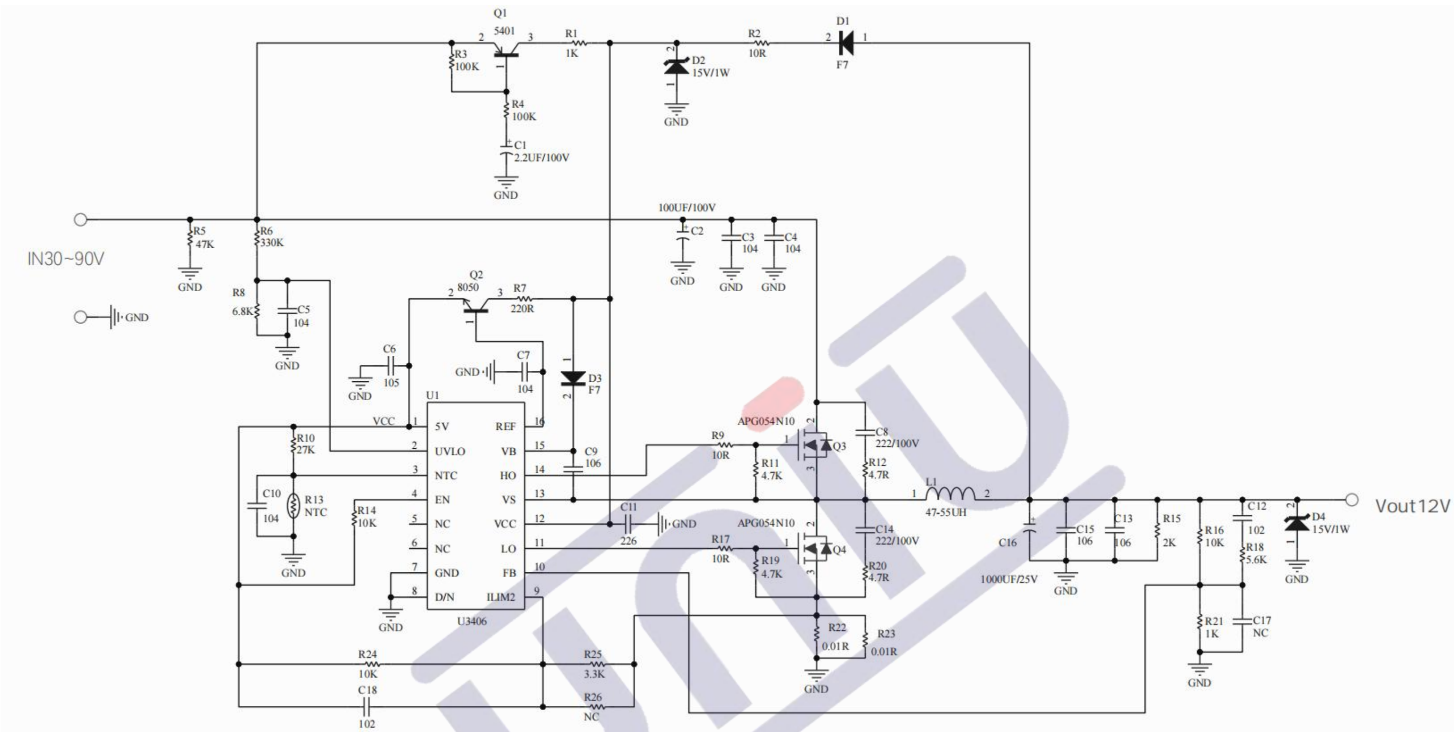
- Device Temperature Grade 1:–40°C to +125°C Ambient Temperature Range
- Versatile Synchronous Buck DC/DC Controller
  - Wide Input Voltage Range of 9.5V to 400V
  - Adjustable Output Voltage From 1.25V to 280V
  - Voltage-mode Control With Line Feedforward
- Three-stage frequency conversion
- 60ns Minimum On-Time for High V_{IN} / V_{OUT} Ratio
- 180ns Minimum Off-Time for Low Dropout
- 1.1V Reference With ± 1% Feedback Accuracy
- 8.5V Gate Drivers for Standard V_{TH} MOSFETs
  - 220ns Adaptive Dead-Time Control
  - 2A Source and 2.5A Sink Capability
- Inherent Protection Features for Robust Design
  - Hiccup-Mode Overcurrent Protection
  - Input UVLO With Hysteresis
  - VCC and Gate-Drive UVLO Protection
  - Thermal Shutdown Protection With Hysteresis
- 16-Pin SOP Package With Wettable Flanks
- Create a Custom Design Using the U3406 With UNI-SEMI ® Power Designer

■ Device Information(1)

Part Number	Package	Body Size (Nom)
U3406	SOP(16)	10mm × 6.3mm

(1) For all available packages, see the orderable addendum at the end of the data sheet

▪ Simple application diagram



■ Output Power Table

Part Number	Package	VIN	IO+/IO-	OUT
U3406	SOP-16	9.5~400V	2A/2.5A	ADJ

Note:

1.Default for Buck Converter Application

2.The practical output power is determined by the output voltage and thermal condition

■ Description (continued)

The U3406 voltage-mode controller with line feedforward drives external high-side and low-side N-channel power switches with robust 8.5V gate drivers suitable for standard-threshold MOSFETs. Adaptively-timed gate drivers with 2A source and 2.5A sink capability minimize body diode conduction during switching transitions, reducing switching losses and improving thermal performance when driving MOSFETs at high input voltage and high frequency. The U3406 can be powered from the output of the switching regulator or another available source, further improving efficiency.

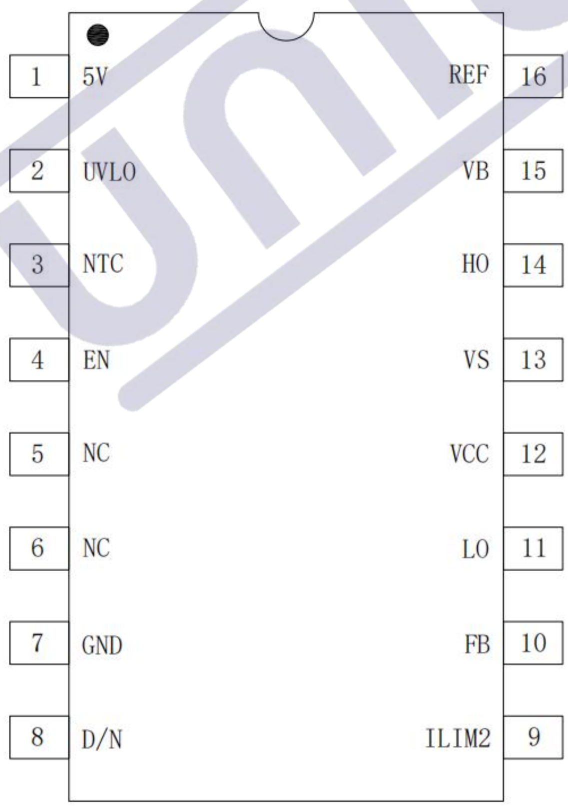
Additional features of the U3406 include a configurable soft start, an open-drain power-good monitor for fault reporting and output- monitoring, monotonic start-up into prebiased loads, integrated VCC bias supply regulator and bootstrap diode, external power supply tracking, precision enable input with hysteresis for adjustable line undervoltage lockout (UVLO), hiccup-mode overload protection, and thermal shutdown protection with automatic recovery.

The U3406 controller is offered in a 10mm × 6.3mm thermally enhanced, 16-pin SOP package with additional spacing for high-voltage pins and wettable flanks for optical inspection of solder joint fillets.

■ Pin Configuration and Functions

RGY Package 16-Pin SOP With Wettable Flanks

Top View



● Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the -20°C to 80°C junction temperature range unless otherwise stated.VIN=48V,VCC=12V,VEN/UVLO=5V,unless otherwise stated(1)(2)

Item	Parameter	Test Conditions	Min	Typ	Max	Unit
Input Supply						
V_{CC}	Operating input voltage range	I_{VCC} ≤ 10mA at V_{VIN} =12V	10	—	25	V
$I_{Q\text{-}RUN}$	Operating input current, not switching	$V_{EN/UVLO}$= 5V,	—	1.8	2.1	mA
$I_{Q\text{-}STBY}$	Standby input current	$V_{EN/UVLO}$= 5V	—	1.75	2	mA
$I_{Q\text{-}SDN}$	Shutdown input current	$V_{EN/UVLO}$= 0V, V_{VCC} < 1V	—	13.5	30	μA
REF/VCC Regulator						
V_{REF}	REF regulation voltage	V_{CT1} = 0 V, 24V ≤ V_{VIN} ≤ 100V, 0 mA < I_{VCC} ≤ 20 mA	—	5	—	V
$I_{SC\text{-}LDO}$	REF short-circuit current	VREF = 0 V VCC=12V	—	50	—	mA
$V_{VCC\text{-}UV}$	VCC undervoltage threshold	V_{VCC} rising	—	8.5	—	V
Enable And Input UVLO						
V_{EN}	Standby to operating threshold	$V_{EN/UVLO}$ rising	—	1	—	V
$I_{EN\text{-}HYS}$	Standby to operating hysteresis	$V_{EN/UVLO}$ = 1.5 V	9	10	11	μA
FB Reference						
V_{REF}	FB reference voltage		—	1100	—	mV
AVOL	DC gain		—	94	—	dB
GBW	Unity gain bandwidth		—	5	—	MHz
Current renferance						
Vlimt2	I limit2 Referance Voltage	VCC=12V	—	1	—	V
Oscillator						
F_{SW1}	Oscillator Frequency – 1	VIN=50V	—	55	—	kHz
PWM Control						
$t_{ON(MIN)}$	Minimum controllable on-time	V_{BST} – V_{SW} = 7 V, HO 50% to 50%	—	160	—	ns
$t_{OFF(MIN)}$	Minimum off-time	V_{BST} – V_{SW} = 7 V, HO 50% to 50%	—	132	—	ns
DC_{55kHz}	Maximum duty cycle	F_{SW} = 55kHz, 6 V ≤ V $_{VIN}$ ≤ 60 V	—	70%	—	—
Gate Drivers						
I_{HOH} , I_{LOH}	HO, LO source current	V_{BST} – V_{SW} = 7V, HO=SW,LO=AGND	—	2.0	—	A
IH_{OL}, I_{LOL}	HO, LO sink current	V_{BST} – V_{SW} = 7 V, HO=BST,LO=VCC	—	2.5	—	A
Thermal Shutdown						
T_{SD}	Thermal shutdown threshold	T_J rising	—	175	—	°C
$T_{SD\text{-}HYS}$	Thermal shutdown hysteresis		—	20	—	°C

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

(2) The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) as follows: $T_J = T_A + (P_D \cdot R_{\theta JA})$ where $R_{\theta JA}$ (in °C/W) is the package thermal impedance provided in Thermal Information.

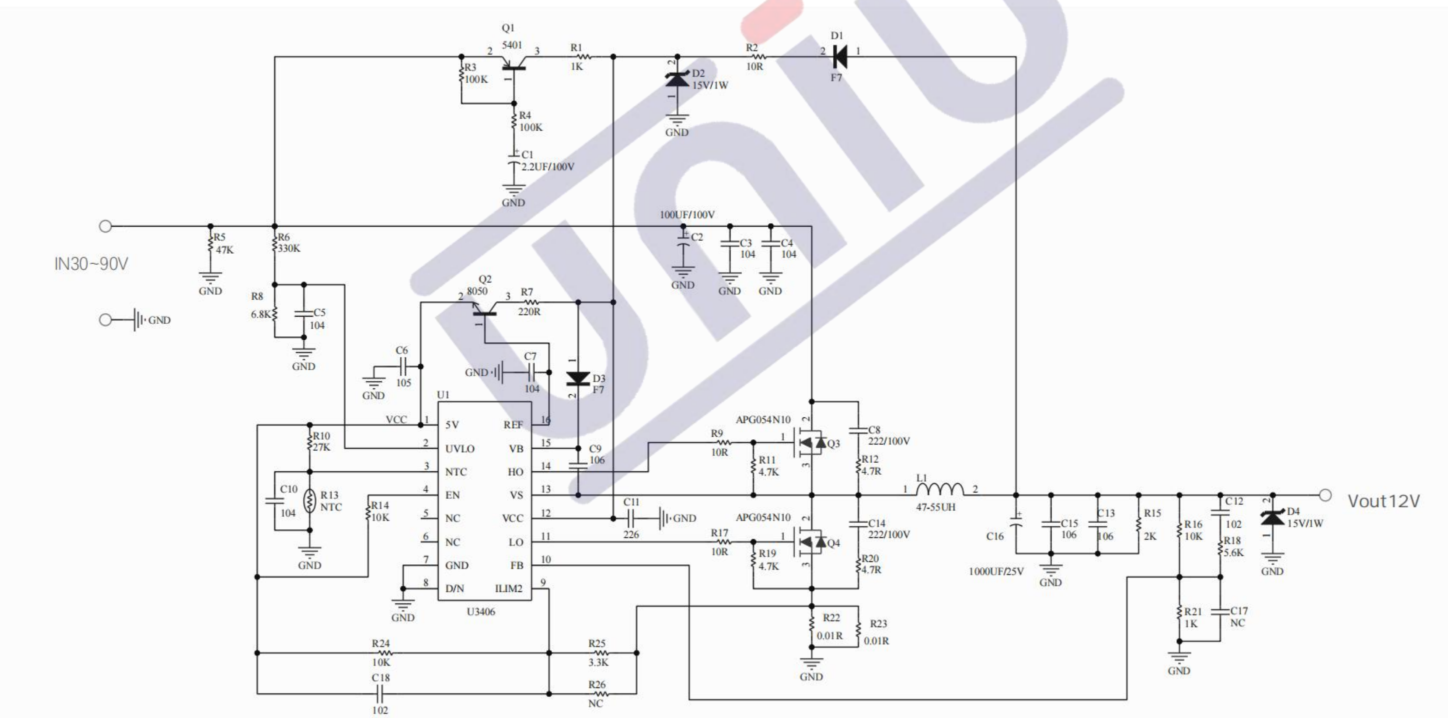
● Switching Characteristics

Typical values correspond to TJ = 25°C

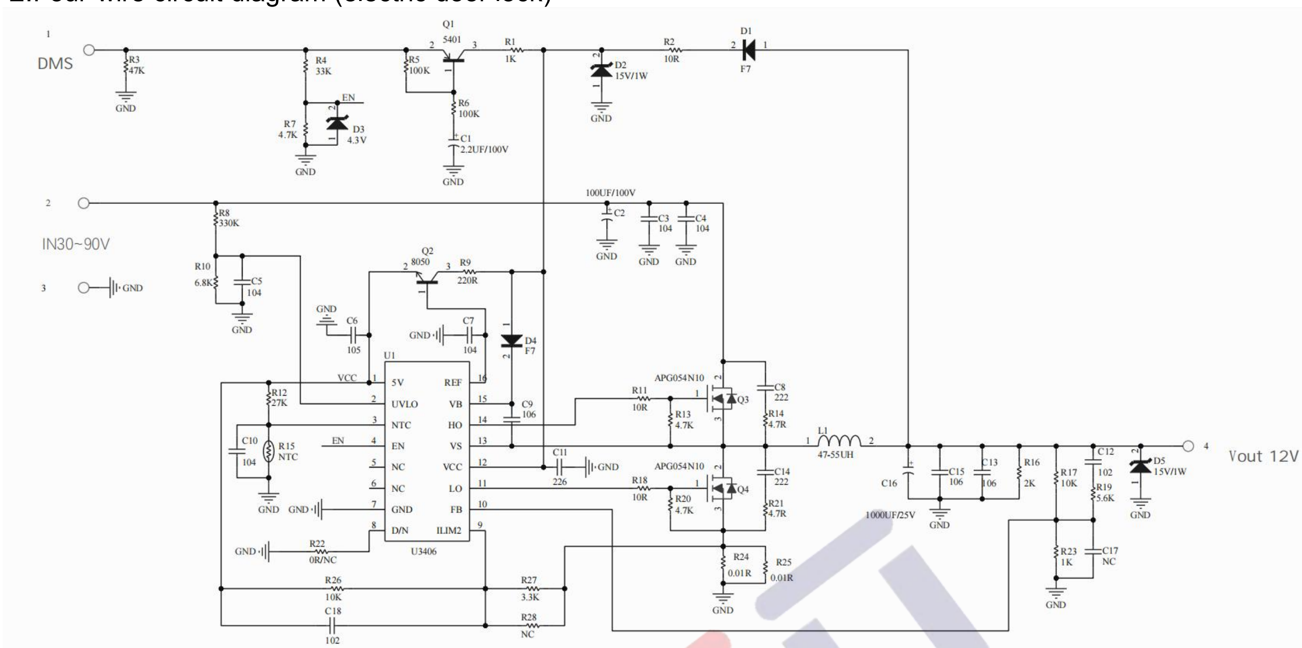
Item	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{HO-TR} T_{LO-TR}	HO, LO rise times	$V_{BST} - V_{SW}$ = 7 V, C_{LOAD} = 1 nF, 20% to 80%	—	25	35	ns
T_{HO-TF} T_{LO-TF}	HO, LO fall times	$V_{BST} - V_{SW}$ = 7 V, C_{LOAD} = 1 nF, 80% to 20%	—	—	25	ns
T_{HO-DT}	HO turn-on dead time	$V_{BST} - V_{SW}$ = 7 V, LO off to HO on, 50% to 50%	—	300	—	ns
T_{LO-DT}	LO turn-on dead time	$V_{BST} - V_{SW}$ = 7 V, HO off to LO on, 50% to 50%	—	300	—	ns

■ Typical Application

APP1:Three-wire circuit diagram(no electric door lock)



APP2:Four-wire circuit diagram (electric door lock)

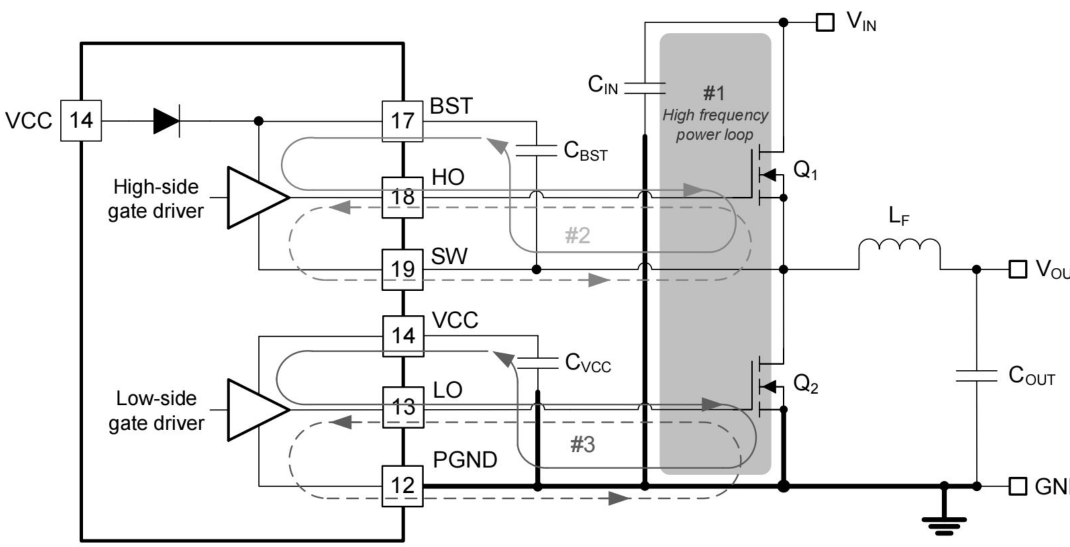


■ Layout

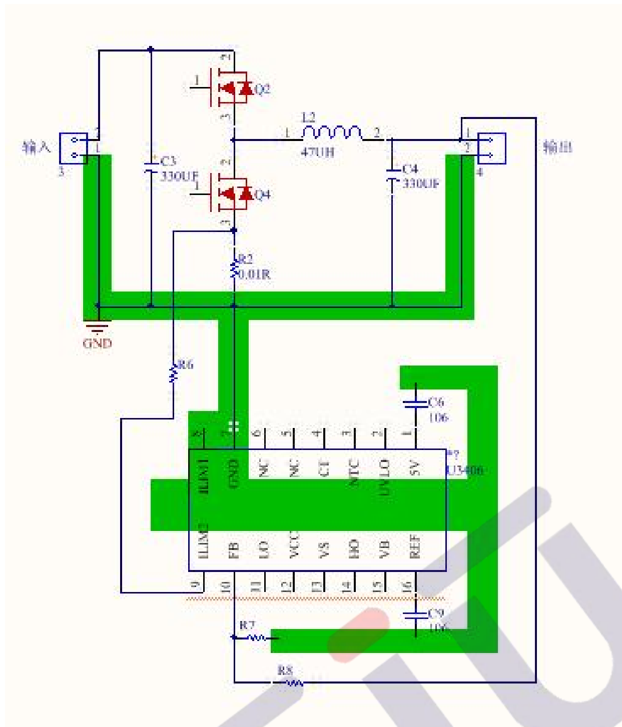
● Layout Guidelines

Proper PCB design and layout is important in a high-current, fast-switching circuits (with high current and voltage slew rates) to assure appropriate device operation and design robustness. As expected, certain issues must be considered before designing a PCB layout using the U3406.The high-frequency power loop of the buck converter power stage is denoted by #1 in the shaded area of Figure 70. The topological architecture of a buck converter means that particularly high di/dt current flows in the components of loop 1, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing its effective loop area. Also important are the gate drive loops of the low-side and high-side MOSFETs, denoted by 2 and 3.

DC/DC Regulator Ground System With Power Stage and Gate Drive Circuit Switching Loops



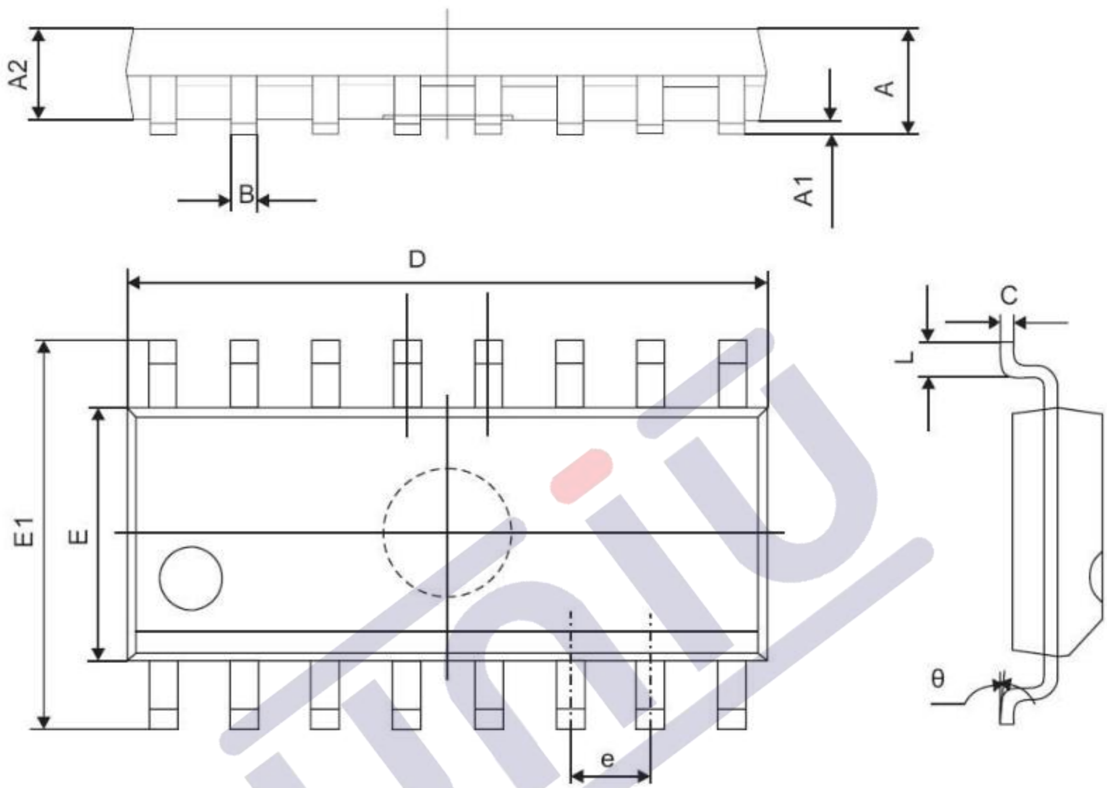
Three wire step-down circuit ground Layout reference.



■ Mechanical Packaging and Orderable

● Mechanical Packaging

SOP-16



（mm）

Symbol	Dimensions In Millimeters	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
B	0.330	0.510
C	0.190	0.250
D	9.800	10.000
E	3.800	4.000
E1	5.800	6.300
e	1.270(TYP)	
L	0.400	1.270
θ	0°	8°

1、版本记录

DATE	REV.	DESCRIPTION
2022/09/28	0.1	首次发布
2023/10/08	0.2	更新应用原理图
2023/11/12	0.3	优化参数及应用原理图
2023/12/30	V0.4	优化参数及功能
2024/5/15	V0.5	优化延时时间

2、免责声明

浙江宇力微新能源科技有限公司保留对本文档的更改和解释权力，不另行通知!

客户在下单前应获取我司最新版本资料，并验证相关信息是否最新和完整。量产方案需使用方自行验证并自担所有批量风险责任。未经我司授权，该文件不得私自复制和修改。

产品不断提升，以追求高品质、稳定性强、可靠性高、环保、节能、高效为目标，我司将竭诚为客户提供性价比高的系统开发方案、技术支持等更优秀的服务。

3、联系我们

浙江宇力微新能源科技有限公司
总部地址：绍兴市越城区斗门街道袍渎路25号中节能科创园45幢4/5楼
电话：0575-85087896（研发部）
传真：0575-88125157
E-mail:htw@uni-semic.com

无锡地址：江苏省无锡市锡山区先锋中路6号中国电子（无锡）数字芯城1#综合楼503室
电话:0510-85297939
E-mail:zh@uni-semic.com

深圳地址：深圳市宝安区西乡街道南昌社区宝源路泳辉国际商务大厦410
电话：0755-84510976
E-mail:htw@uni-semic.com